HARMONICS ANALYSIS OF FOUR SWITCH THREE PHASE INVERTER

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ABSTRACT

In the viewpoint of reliability implication and cost effectiveness of three phase inverter, there should be less device count in inverter topology and fewer losses in the semiconductor switches. The earlier reported less device count topology by many research groups are facing the problem of Total Harmonic Distortion (THD). The imperfect design value of DC link capacitor is the main reason of Harmonic Distortion (THD) problem. The ripple in the dc link voltages of Voltage Source Inverter (VSI) is leads to additional harmonics distortion. This paper present the simulative view of minimization of the harmonic reduction in proposed topology using improved DC link capacitor. The said approach is verified using PSIM (Power Simulator) software.

1. INTRODUCTION

The wide application area of AC machine in the industries and home application such as pumps, conveyors, machine tools, centrifugal machines, presses, elevators, and packaging equipment etc require the cost effective and low losses variable frequency drive. The conventional variable frequency drive using six controlled switches does not prove its applicability in the chaining era of technology transformation, Hence electronic drives have not reaches to the consumer market due to their high initial cost.

In recent year the effort is made to minimize the conventional six switches topology into five to four switches by various research groups [1- 5, 14]. The Frede Blaabjerg, et al proposed an adaptive space vector modulation (ASVM) approach to compensate the dc-link voltage ripple in an inverter topology [1]. Similar work was carried out by Ching-Tsai Pan et al for a low cost voltage-fed current controlled inverter for induction motor drives [2], Heinz W. Van Der Broeck et al investigate the three-phase induction machine drive with a component minimized voltage-fed inverter under different control options [3]. J. F. Eastham et al reported the various power inverter topologies [4] and Brian A. Welchko and Thomas A. Lipo [5] reported a novel current source control method for a three-phase induction machine. T. D. Dongale et al [14] reported the simulative view for minimization of active switches in conventional six switch topology. The earlier reported less device count topology by many research groups are facing the problem of Total Harmonic Distortion (THD). The imperfect design value of DC link capacitor is the main

reason of Harmonic Distortion (THD) problem. The ripple in the dc link voltages of Voltage Source Inverter (VSI) leads to additional harmonics distortion. This paper presents the simulative approach for variable frequency drive using PSIM software with improved DC link capacitor value for minimum Total Harmonics Distortion (THD). The proposed variable frequency drive is poles apart from main stream three-phase drive system because it is only uses four controlled switches.

The proposed system gets good speed regulation and adequate efficiency with minimum switches. This paper also proposes the novel technique for speed control of AC induction machine using four controlled switches than that of the conventional topology [6-14]. The main objective of this proposed topology is to reduce controlled switches and freewheeling diode count from mainstream Voltage Source Inverter (VSI) topology [14]. The cost reduction is also prime objective of this work using reducing controlled switches. It is also reduced the number of driver circuits form the conventional Voltage Source Inverter (VSI) topology [1]. Due to lower cost and adequate performance of the proposed topology will breakthrough consumer market into new perspectives. The rest of the paper proceeds as follows, at the outset, section I is focused on introduction of proposed topology. Section II describes the actual method of simulation by using PSIM software and finally the section III and IV describes the result and conclusion respectively.

2. PROPOSED TOPOLOGY AND ITS DESCRIPTION

The detail study of proposed topology is carried out by using PSIM (*Power SIMulator*) software. The fig.1 presents the proposed topology of 3 phases VFD using only four controlled switches. For the simulation Insulated Gate Bipolar Transistor (IGBT) is used as controlled switch [14]. The Switches are controlled using sinusoidal PWM technique. At any instance only two phases are conducting. The conduction of these phases is about 240° of a cycle. Here Induction motor is considered as load. The output voltages are defined by the gating signals of the two leg switches and by the dc-link voltages [1, 14]. The actual simulative implementation is shown in fig.1 and the gating sequence of this proposed technique is shown in table I. [14]

Table I: The Gating Sequence of Proposed Topology [14]

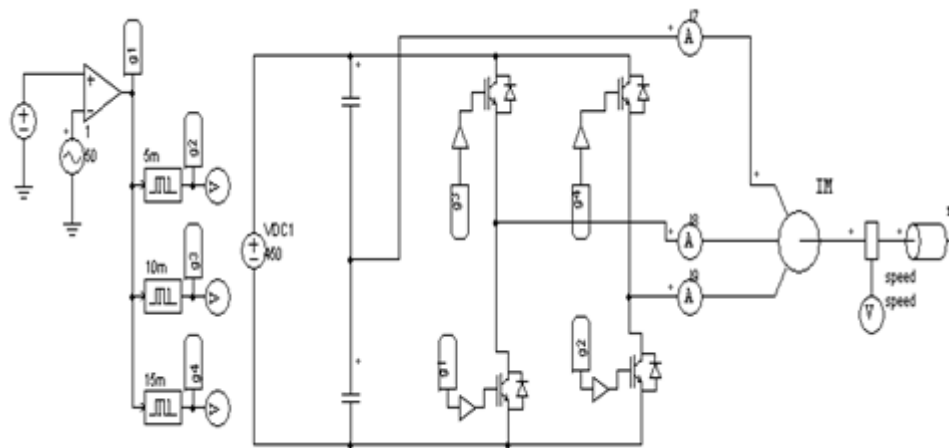| Switches on at Given Phases	
V1	V2
V1	V3
V4	V2
V4	V3

Figure 1: Proposed Topology of Three Phase Variable Frequency Drive (VFD) Using Four
Controlled Switches [14]

3. RESULTS

From the simulation it is clearly seen that, there is good agreement between proposed four switch inverter topology and conventional six switches inverter topology. The fig. 2 shows the phase current waveform of three phases as I_A, I_B, and I_C respectively and fig 4 shows the phase voltage of phases V_{BC}, V_{AC} and V_{AB} respectively. The current waveform is not good enough compared to conventional three phase current waveform. The current and speed distribution relation during motor start-up is shown in fig. 4. The large settling time is observed in fig. 4, it is probable due to the less number of controlled switches. [14]
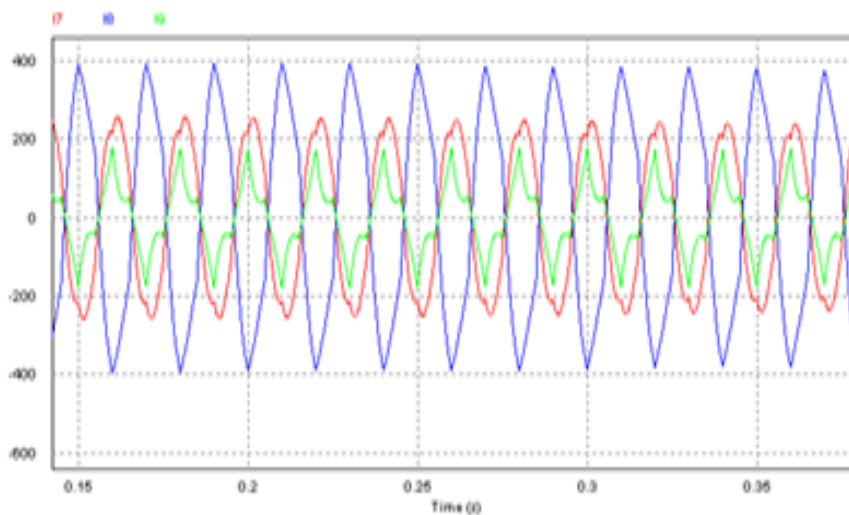

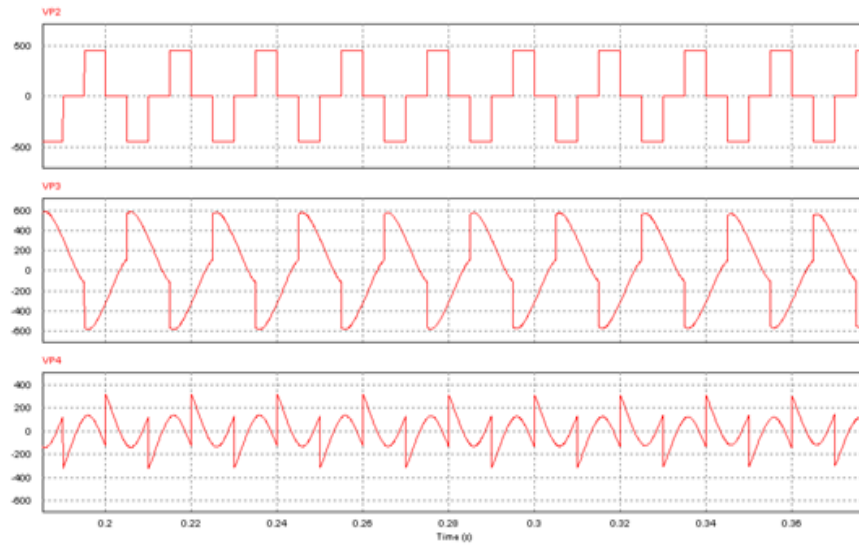Figure 2: Three Phase Current Waveform of I_A, I_B and I_C. [14]

Figure 3: Phase Voltages of Phases V_{BC}, V_{AC} and V_{AB} respectively [14]
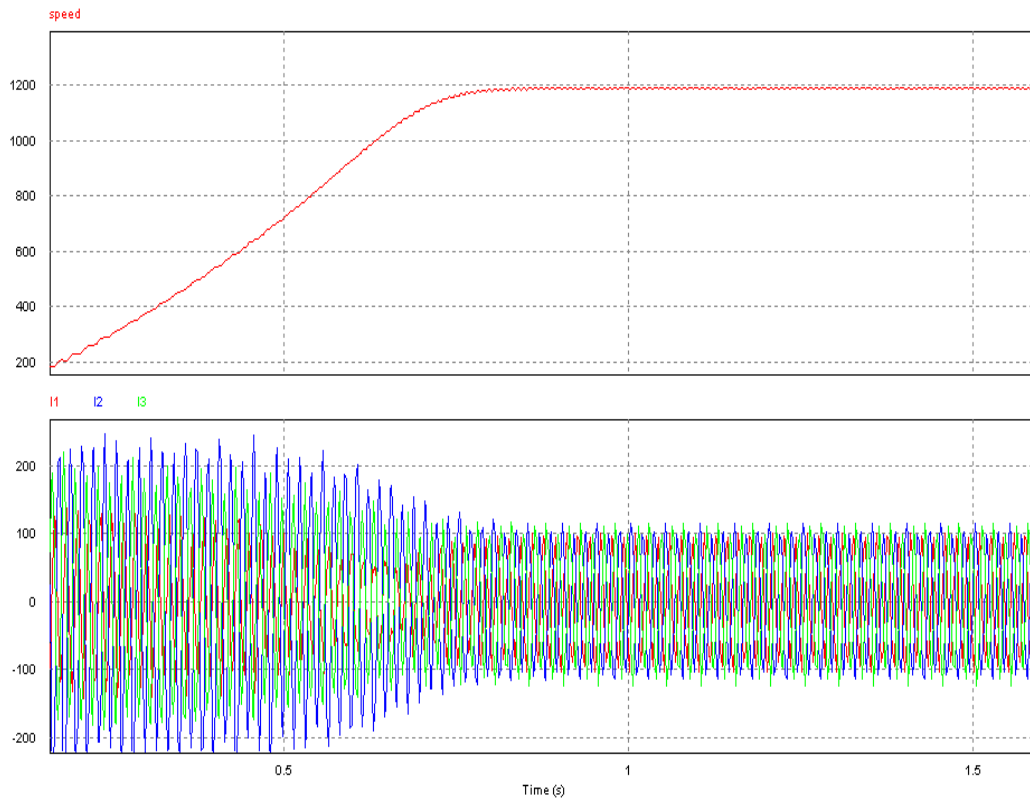

Figure 4: The Simulation Results of Induction Machine Drive System during Motor Start-Up. The Upper Figure Shows the Speed Regulation of Induction Motor and Lower Figure Shows Current Waveform of Induction Motor. [14]
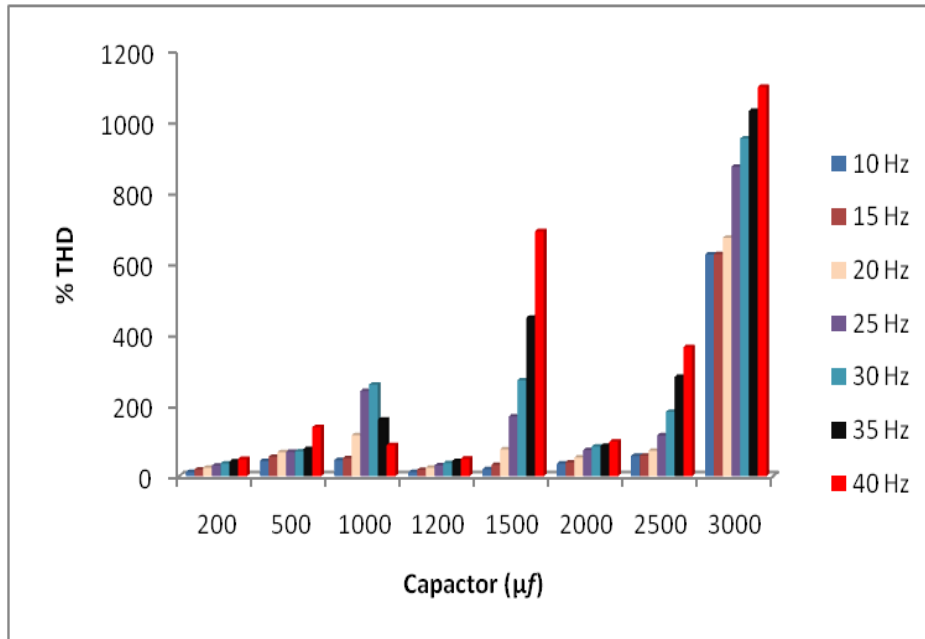
Figure 5: Total Harmonic Distortion Factor of Proposed Inverter Topology. The THD is Increases as Frequency and Capacitor Value Increases. It is optimum at 1200 μf DC Link Capacitor Value.

The Total Harmonic Distortion factor (THD) is presented in Table II and fig.5. The total harmonic distortion factor (THD) can be used as an optimization factor for Voltage Source Inverter (VSI) in general [10]. The minimum Total Harmonic Distortion factor can be found in the range 1200 μf capacitance value. The THD maximum at the DC link capacitor 3000 μf and it is increases as frequency and DC link capacitor value increases. The present inverter topology presents the four controlled switches; due to fewer devices in action odd harmonics and ripple in the dc link voltage are seen. To overcome this problem an additional filtering in the dc link is required or another solution is used an adaptive space vector modulation (SVM) algorithm. [1, 14-17].

Table II: The Total Harmonic Distortion (THD) of Proposed Topology

Frequency (f)	10 Hz	15 Hz	20 Hz	25 Hz	30 Hz	35 Hz	40 Hz
DC Link Capacitor (µf)	THD (%)	THD (%)	THD (%)	THD (%)	THD (%)	THD (%)	THD (%)
200	12.10	18.9	24.4	30.21	36.45	42.23	48.71
500	43.53	54.84	67.87	68.83	70.52	77.46	138.85
1000	45.75	51.11	115.95	241.20	258.91	160.31	87.95
1200	11.92	18.07	24.40	30.75	37.18	43.22	49.70
1500	20.31	32.40	76.50	169.28	271.42	448.17	692.39
2000	35.90	39.39	53.07	73.86	84.40	86.24	97.90
2500	57.65	58.30	72.50	115.62	182.32	281.37	365.13
3000	626.71	628.00	673.96	874.98	954.61	1032.99	1100.44

4. CONCLUSION

This paper presents a simulative approach for variable frequency drive and along with the novel control method for a three-phase induction machine using only four controlled switches with reduction in Total Harmonic Distortion factor (THD). The low cost of the present topology make the new paradigm in the inverter design. The harmonic distortion is reduced by employing the correct DC link capacitor. For the present case the DC link capacitor is about 1200 µf. Fluctuate phase current nature of proposed topology is a still alive problem in hardware implementation. This problem arises because of less number of active switches used in the proposed topology.

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