Key technologies for distributed wireless networking and ECMA-368 MAC layer LSI design challenges

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Abstract. Distributed wireless networking enables opportunistic operation of personal area networks (PANs). In PAN scenario, it is desirable that each device can establish a wireless connection among devices near by, without a help of access point (AP) or central coordinator. Distributed Media Access Control (MAC) is one of the key technologies enabling distributed wireless networking, and WiMedia Alliance worked on the specification of distributed wireless networking technologies. The specifications developed by WiMedia Alliance were standardized published as ECMA-368 – High Rate Ultra Wideband PHY and MAC Standard, and ECMA-369 – MAC-PHY Interface for ECMA-368. This paper introduces the technology overview of ECMA-368 MAC and the MAC LSI design challenges. This MAC LSI is intended to offer a generic communication platform to meet various application needs, and was certified to be compliant to the specification by WiMedia. The MAC design includes not only standardized protocol set, but also some additional enhancement features to achieve better performance or to meet certain application requirements.

Keywords: WiMedia, UWB, MAC, ECMA-368, ECMA-369, adhoc network, PAN, Superframe, Beacon Period, DRP, PCA, Block ACK, LSI, ECMA-387.

1 Introduction

Wireless PAN System is one of the candidate technologies to form opportunistic ad-hoc network and transmit wideband data among personal devices. WiMedia Alliance worked on the UWB based high-speed PAN system specification utilizing OFDM based PHY providing up to 480Mbps, and distributed controlled MAC mechanisms [1] [2]. The MAC/PHY specification has been further standardized in ECMA TC48 and published as ECMA-368 – High Rate Ultra Wideband PHY and MAC Standard. The MAC technology specified by this standard contains many key technologies that enable distributed media access for personal area networks. As well as technology specification, implementation of the technology is another key challenging factor to realize the wireless PAN systems. The MAC technology is implemented in LSI. Based on the careful review of requirements, effective, viable, and extendible architecture design is vital in designing MAC LSI.

In this paper, overview of ECMA-368 MAC protocol is introduced firstly, in order to capture the key technologies enabling distributed wireless networking. Further, some general requirements for the MAC implementation are discussed, and designed LSI architecture and features are described. We named this MAC LSI "Magnicours". Magnicours is aiming at the embedded chip solution for wireless PAN in general, and tries to handle high bandwidth signal with lower power consumption, to meet the general wireless PAN application requirements. We have done some measurements using this LSI, and some of the measurement results are also summarized at the later section. As discussed later, it is expected that Magnicours design is also applicable to other systems other than UWB.

2 ECMA-368 MAC protocol

ECMA-368 MAC is a packet based access protocol, designed to deliver the scheduled channel access in distributed coordination environment, with additional accommodation of contention based access [4]. Some features characterizing ECMA-368 MAC are briefly introduced in this section.

2.1 Frame format

In ECMA-368, all signals are transmitted in forms of "frame" (packet). ECMA-368 MAC frame format is shown in figure 1. MAC header is placed inside of the PLCP header field where the strong channel coding is adopted to make it robust against errors. By putting MAC header inside the PLCP field, important header information can be delivered to the receiver with higher probability. The header field is followed by the 16 bit Header Check Sequence (HCS) that is used to detect errors in this field. 16 bit error detect sequence is relatively short, and the implementer should include additional error detect mechanism to mitigate false-positive error at the MAC layer.
The maximum PSDU (PHY Service Data Unit) size is 4,095 octets. MSDUs (MAC Service Data Units) may be aggregated into a PSDU and may be transported over a single frame. This frame is called aggregated MSDU frame.

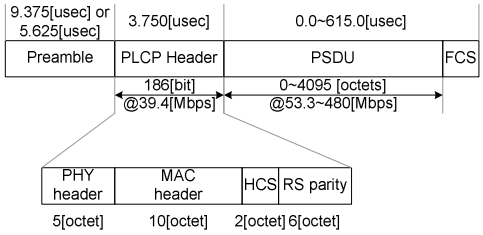

Fig. 1. Frame format

2.2 Superframe structure

ECMA-368 MAC defines the basic time controlling unit called Superframe. Superframe is a constant duration of 65,536 [usec]. Superframe is composed of 256 MASs (Media Access Slots). The MAS duration is 256 [usec], and it is a basic unit for the channel time allocation. The channel time utilization is defined by the MAS type that is categorized as one of the following three types.

- BP: The duration when only beacon frames are transmitted. All other types of frames can not be sent during this period.
- DRP: Reserved time slots for the DRP owner to accommodate the scheduled channel access.
- PCA: The time slots which are open for the prioritized contention access. Devices contend with CSMA/CA mechanism to get a channel access.

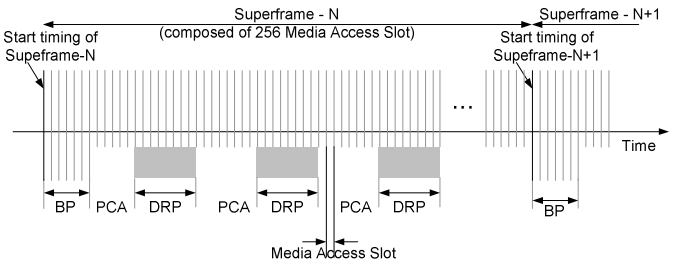

Fig. 2. Superframe structure

2.3 BP (Beacon Period)

Since there is no central coordinator in the distributed wireless network environment, all the devices needs to announce its service availability in some way. In ECMA-368, this has been done through beaconing. All the devices transmit beacon frames in the BP of a Superframe. Beacon Period is further divided into time units called beacon slots. In each beacon slot, one beacon frame is transmitted. Each device tries to find out the right beacon slot to transmit beacon frames, so that the transmitted beacon frame does not collide with beacon frame of other devices [8]. It is important to operate the collision avoidance among beacon frames since the beacon frame is transmitted without acknowledgement and the transmitter may not know if the frame is received by the neighbor devices correctly. The collision avoidance is controlled by announcing beacon slot occupancy status [4]. Each device announces which beacon slot is occupied by neighbor's beacon frame, and the device transmitting beacon frame chose its beaconing slot from one of the beacon slot which is reported as vacant slot from all of its neighbors.
Devices receiving beacon frames can obtain the device/network availability near by, and beacon frames are also used to signal most of the control information. For instance, DRP establishment is signaled using DRP IE (Information Element) contained in the beacon frame.

2.4 DRP (Distributed Reservation Protocol)

DRP provides TDMA-like reserved channel access and is intended to accommodate streaming applications. Even without a central coordinator, reservation access can be achieved since all the devices conform to the DRP negotiation and utilization rules.
In order to establish DRP, devices need to negotiate among neighboring devices. Once the negotiation for setting up DRP succeeds, devices can utilize the established DRP MASs (time slots). Once it is established, DRP MASs are utilized exclusively for the reservation owners. All other devices other than the DRP owners shall be silent during the DRP MASs. Although DRP owners are allowed to use DRP, all the frame exchange sequences shall be terminated within the DRP MASs.

DRP assignment pattern will affect required buffer sizes and data delivery delays. In order to deliver the fair channel access opportunities, there are certain rules for obtaining DRP reservation slots. In general, frequent MAS allocation helps in minimizing buffer requirements, whereas smaller MAS block results in larger overhead due to a fragmented utilization of the channel time [6].

2.5 PCA (Prioritized Contention Access)

The MASs other than BP or DRP can be utilized as PCA when the channel access is open for all the PCA capable devices utilizing contention access. PCA in ECMA-368 is similar to EDCA, defined in IEEE 802.11 wireless LAN, utilizing multiple prioritized contentions based on Carrier Sense Multiple Access with Collision Avoidance (CSMA/CA) [11]. PCA assumes that the transmitter has 4 parallel queues for each access category, and runs random backoff timers in parallel to gain a channel access. Unlike IEEE 802.11 wireless LANs, PCA imposes that the frame transmission needs to be controlled to be accommodated within the PCA time slots. That is, PCA requires a strict TDMA based time management, whereas it offers a contention based channel access [7]. In case of PCA, the use of RTS/CTS procedure is preferred to keep the channel capacity higher when the network is overloaded. By utilizing DRP and PCA together, devices can provide stable and efficient services to the applications while minimizing the channel occupancy.

2.6 Frame transmission sequence

Frames may require acknowledgement from the receiver, to offer a reliable frame transmission. 2 kinds of ARQs are defined. The first one is a use of immediate ACK, where ACK frames are sent back immediately after the each data frame reception. This is easy to operate, but the overhead is large, especially when the frames are transmitted at higher PHY rates.

The other one is a use of Block ACK. Block ACK is sent back to the transmitter only when the frame with Block ACK request is received. In this case, ACK frames are not required to be sent back frequently,

and contribute a lot to reduce the overhead. Data frames can be transmitted successively, which is called "bursting", with smaller inter frame spacing called MIFS (Minimum Inter Frame Space).

When used with RTS/CTS procedure, TXOPs can be obtained assuming that the data frames will be transmitted using bursting, and set the duration field to the end of the last burst data frame.

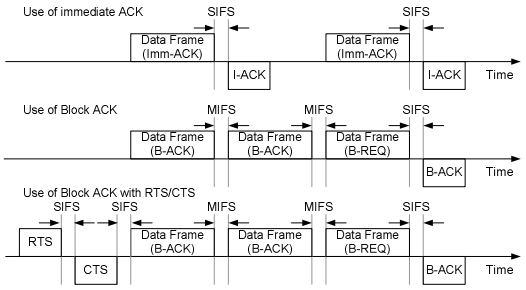

Fig. 3. Frame exchange sequence example

3 Determination of the requirements for MAC implementation

There are many different requirements for wireless communication interfaces from the application and/or client device point of view. Some devices only have limited hardware resources and can not afford handling huge signal processing for access control at the client CPU. These kinds of devices usually intend to conserve power. In contrast, some devices require precise control for QoS delivery which is vital for real time AV stream handling. Some application may need to deliver traffics to multiple devices at the same time. It is also important to note that the footprint for the chip design affect the cost performance. Following items are some of the important requirements to be considered when the MAC LSI is designed in general.

- Reduction of signal processing load at the client
- High bandwidth signal processing
- Low power consumption
- Efficient utilization of hardware resources
- Extendibility of the platform

Considering the typical use case of the high-speed wireless PAN system, in particular, we have set the following aims for the application of the MAC LSI.

- Aim at the installation to the embedded system
- Aim at video straming type of application

These aims derive certain priorities to the general requirements listed above.

4 Architecture design

Taking into account the general requirements for MAC implementation described above with a certain priority, we have chosen the architecture of the LSI (Magnicours) carefully to meet many of these requirements. The designed MAC is composed of the following three major building blocks.

- Client driver software:
- Embedded CPU and software:
- Custom hardware logic:

The functionality mapping is depicted below.

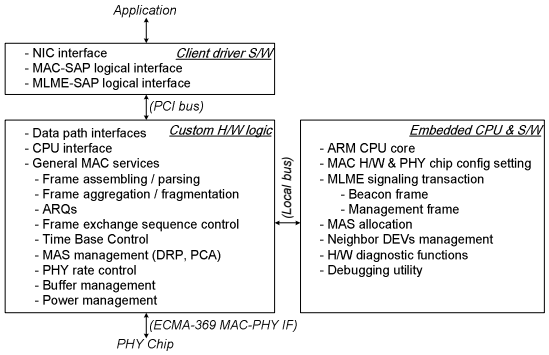

Fig. 4. Functional blocks of the MAC design

The custom hardware logic portion consists of the functional blocks depicted in the figure 5. Most of the ECMA-368 MAC services are processed at the "event driven framing and buffer handling engine" and "time driven event processing engine". In order to achieve both the higher bandwidth signal processing and lower power consumption, most of the data path should be handled by the hardware logic [10]. Magnicours handles all the data path transaction with custom hardware logic portion only. This is one of the distinctive design rationales of Magnicours. Since one of the aims of our design is to offer reliable streaming application services with light weight client operation, Magnicours has rather large internal memory for data buffers.

The extendibility and the reusability of the design are also important for LSI IP. To maintain these capabilities, the module interfaces among "Embedded CPU", "Interface from/to client", and "ECMA-368 MAC service engine" in the figure 5 are simplified as much as possible so that some of them can be replaced by the updated modules with minimal effect to the other modules.

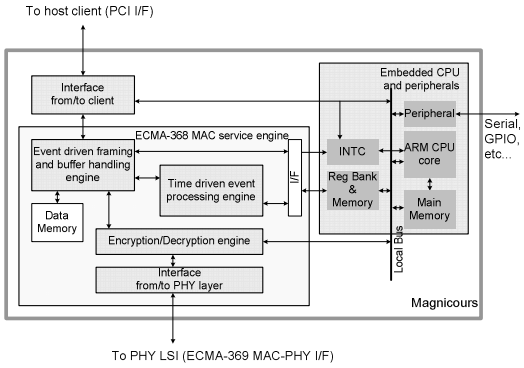

Fig. 5. Hardware structure of Magnicours

5 LSI specification

Physical specification of the Magnicours is summarized in the table below.

Table 1. Summary of the Magnicours specification

Silicon process	TSMC 90LP TSMC library
Die size	4.5mm x 4.5mm
Package	19mm x 19mm TBGA484
Logic size	0.7MGate for ECMA-368 MAC service engine and interface circuits, 0.3MGate for CPU core,

SRAM for CPU	2Mbit for instruction, 1Mbit for data processing,
SRAM for data buffer	2.5Mbit (TX/RX buffer)
Clock	Ext.In 16.5MHz (20ppm), Internal max. 66MHz
Interface	ECMA-368 MAC-PHY I/F, PCI IF (Cardbus I/F),

Since this LSI itself is not intended for commercial services directly, we have included many redundancies such as test circuits or spare memory spaces so that the LSI can be used for various verifications. The memory size could be reduced once the resource utilization is verified, which results in significant reduction of the footprint. Magnicours also outputs many test pins, which can be also eliminated eventually. The following figure shows the layout (floor plan) and pin I/O of the Magnicours. As can be seen from the figure, the die size reduction is not optimized and there are many room for the size reduction.

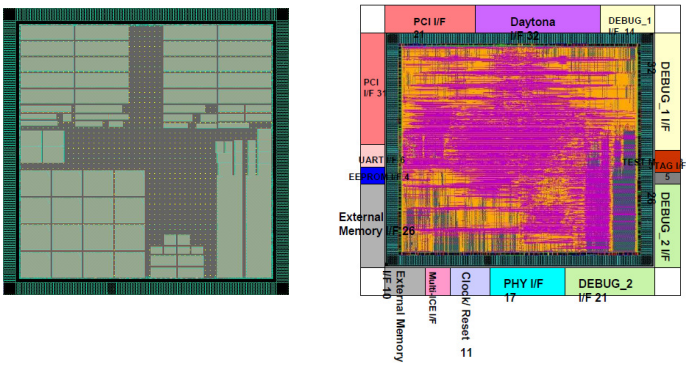

Fig. 6. Magnicours floor plan and pin I/O

The following photos show the Magnicours and the evaluation board. Thanks to the standardized interface, third party PHY LSI can be connected via the MAC-PHY interface specified by ECMA-369.

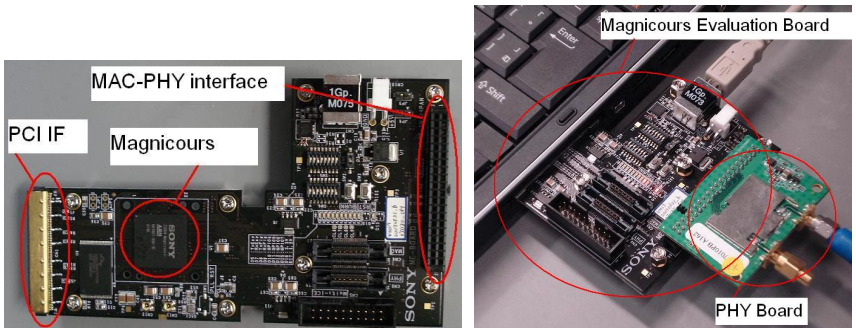

Fig. 7. Magnicours and evaluation board

6 Major functionalities and implementation policies

Some of the functionalities offered by Magnicours and the implementation policies are briefly introduced in this section.

6.1 MAS management

MAS assignment is one of the critical portion of the ECMA-368 MAC protocol. Since the MAS utilization needs to be strictly controlled based on the signaled information over beacon frames, Time Base Control is handled by hardware logic part, based on the information parsed by the embedded software. Once the time allocation schedule is ordered by the software, the hardware modules manage the channel time precisely in autonomous way. This role partitioning contributes to lower the power consumption and keep the extendibility.

6.2 Frame transmission sequence

Frame transmission sequence needs to be determined by the following status at least:

- MAS status: whether the frame is transmitted via DRP or PCA, and how much channel time is available for this transmission.
- PHY data rate: at which PHY rate the frame is to be transmitted.
- Buffer status: pending transmission data amount, number of packets, and reported receiver's buffer availability.
- ARQ status: ARQ mode that is used for this transmission. If the Block ACK is open, data will be transmitted using bursting.

Magnicours is capable of handling both DRP and PCA. Mixed utilization of both access schemes is also possible to serve better performance. Since Magnicours aims at the extendibility for the higher bit rate, the determination of above factors and the frame assembling are processed by the hardware logic part.

6.3 Block ACK

Block ACK contributes a lot to reduce the overhead, although the implementation of Block ACK imposes many challenges. It is necessary to manage the buffer in real time and synchronize the buffer status with its counterpart of the transmission using the ARQ information such as Stream Index, Sequence Number, ACK Bit Map, etc. Since these processing is required for every frame transmission/reception, it is preferable that these transactions are handled with hardware portion again, especially if the LSI aims to offer high bandwidth transmission with lower power consumption. Magnicours handles all the Block ACK transaction within hardware logic part, based on the given status information. When ARQ related synchronization is lost, software will initialize the broken ARQ status and recover the transmission.

6.4 Frame aggregation

Frame aggregation is another promising feature to reduce the overhead at the MAC layer significantly. Although only MSDU aggregation is defined in ECMA-368 MAC, another aggregation method, which is called MPDU aggregation as defined in 802.11n [12], offers better characteristics if the aggregated frame size is larger. In case of MPDU aggregation, Frame Check Sequence is appended per MSDUs, and these MSDUs can be retransmitted independently regardless whether the frame is aggregated or not.

It is also important to note that the maximum PSDU length should be defined longer to aggregate MSDUs efficiently. Although maximum PSDU length for ECMA-368 MAC/PHY is 4,095 octets, it should be defined longer for further enhancements. The framing overhead δ can be calculated as following equation.

$$\delta = \frac{N_B L_P / R}{N_B L_P / R + T_{P1} + (N_B - 1)(T_{MIFS} + T_{P2}) + T_{SIFS} + T_{ACK}}$$

where N_B is a number of bursting frames, L_P is a packet length, R is a PHY data rate for transmission, T_{P1} is a standard PLCP heading duration, T_{P2} is a short PLCP heading duration, T_{MIFS} is a MIFS duration, T_{SIFS} is a SIFS duration, and T_{ACK} is a ACK frame duration.

For instance, if we assume 16 MSDUs (each of them consists of 4,000 octets) transmission using bursting or aggregation at PHY rate of 480Mbps, the overhead percentage varies from 16.4% (when max MSDU size is 4k octet) to 3.6% (when max MSDU size is 64k octet). When higher PHY rate is offered,

the overhead reduction rate will become larger. This means that the frame aggregation technique is very important when designing even higher speed PAN system. Magnicours aims for the higher data rate and better performance extendibility, thus offers both MSDU aggregation and MPDU aggregation, although MPDU aggregation is not specified in ECMA-368 MAC. Further, PSDU length up to 65,535 octets can be handled internally.

6.5 Rate control

PHY offers multiple modulation and coding schemes (MCS) to achieve various data rates [5]. MAC is responsible for selecting which MCS should be used for each data frame transmissions. There are many strategies to control the PHY layer data rate proposed by many researchers [9]. We have implemented the following 3 mechanisms to meet with the various use cases or external restrictions.

- PER observation based algorithm: The MCS is selected observing the PER (Packet Error Rate).
- PER and LQI combination algorithm: The MCS is selected using the outer and inner loop rate control. These loops are controlled based on the PER and reported LQI (Link Quality Indicator) from PHY layer.
- Externally specified rate: The MCS is set to the value specified by the client.

6.6 Power management

Power management protocol is defined as a part of the ECMA-368 MAC protocol. In order to leverage the power management efficiently, the MAC LSI disables and enables PHY chip activity based on the Superframe utilization. Thus, the PHY chip status can be changed frequently even when the data transmission is ongoing. Further, CPU will be disabled when management frame transaction is not required, and most of the clock delivery inside the LSI will be suspended when the clock delivery is not necessary. Clock signal will be delivered only to the modules and memories that are processing signals, as for modules in the ECMA-368 MAC service engine.

6.7 Buffer resource management

Buffer handling is one of the key features for high data rate applications. The system should utilize the memory space efficiently, since the memory size usually affects a lot in terms of the footprint of the LSI. At the same time, flexible queue control is required to meet the broad application requirements. In Magnicours, transmission buffer and reception buffer are shared in a single memory space, and transmission queues are managed per multiple stream index and receiver.

In order to mitigate the effects of Head-of-Line Blocking in case the traffic is delivered to multiple destinations, the buffer resource management function controls the buffer utilization, monitoring the incoming and outgoing traffic streams. The memory space for transmit data buffer and receive data buffer can be adaptively adjusted by the monitored traffic flow. Data traffics up to 15 devices are controlled simultaneously. When the device is delivering data frames to multiple receivers, the transmitting device selects the receiver prior to the frame transmission, so called receiver selection. In typical MAC implementation, receiver selection is handled by the software portion. However, Magnicours handles the receiver selection in the hardware portion inside the LSI, so that the signal processing load at the client software can be reduced. Thus, the client only needs to input the transmitting data to this LSI without taking care of receiver selection.

Some additional buffering flexibility allows the further enhancements by means of cross-layer optimization among applications.

Buffers at the MAC layer can be used for other purposes such as jitter compensation. Since Magnicours may be connected to a simple application engine such as video codec directly, it contains relatively larger size of data memory space, and delivers some additional functionality to compensate jitters of packet arrival. In this use case, the most of the memory space at the receiver are utilized as receive buffer, and can be used for jitter compensation purpose.

Further, the timeout for the data delivery can be set in per MSDU basis, which allows more flexibilities and possibilities for cross-layer optimization.

7 Measurement results

Some measurement of Magnicours MAC LSI has been carried out, and reported in this section.

7.1 MAS management

As described above, MAS utilization is signaled through beacon frames among devices near, and all the devices shall conform to the specified rules. We have tested the implemented protocol using the protocol analyzer. Some MAS utilization results captured by the analyzer are shown in the figure below. It can be seen that all the frame exchange occurs only during the reserved MASs (cited as "Reservation Block" in the figure) for DRP, and does not violate the other MAS spaces that shall be kept clear for the communication among other devices.

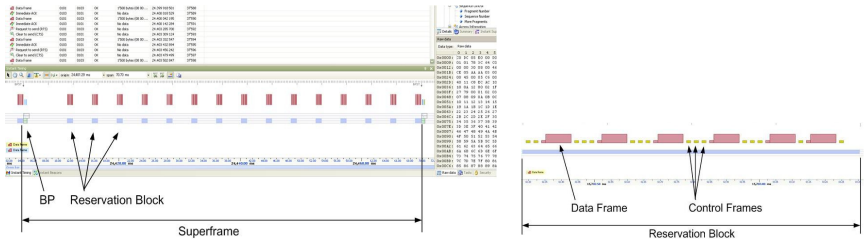

Fig. 8. MAS utilization captured by an analyzer

The MAS utilization conformance test is performed by WiMedia Alliance as a part of certification program. We also passed the conformance test, and the result is listed in WiMedia website.

7.2 Application Throughput

The application level throughput transmitted over this MAC has been measured. Using the bursting transmission with Block ACK and frame aggregation, two transport streams up to 180Mbps (360Mbps = 180Mbps x 2) are constantly accommodated[1].

7.3 Rate control

Adaptive rate control behavior is also observed to verify the implemented algorithms. PHY data rate control example is shown in the Figure 9. The graph on the left side shows the rate control behavior conducted by the computer simulation assuming the time varying channel response due to the multi-path fading. 2 kinds of rate control algorithms (PER observation based algorithm and PER and LQI combination algorithm) are tested by the simulation and the results are shown in this graph. The graph on the right side is a rate control behavior of Magnicours captured by a protocol analyzer in our lab. In this measurement, PER observation based algorithm is activated. It can be observed that the PHY rate is selected to meet the varying channel condition.

[1] With the testbed we developed, host client has a restriction in bus handling and it limits the throughput per stream. The MAC LSI itself has a capability to offer > 1Gbps except the MAC-PHY interface.

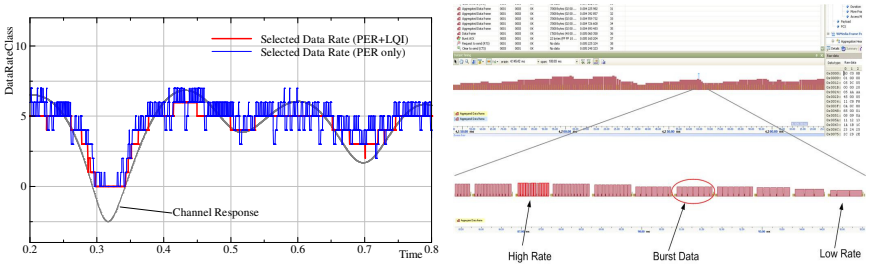

Fig. 9. Rate control behavior conducted by the simulation (left side), and rate control behavior captured by an analyzer (height of the bar represents PHY rate) (right side)

7.4 Power consumption

"How much power will be consumed for the MAC signal processing?" This is one of the difficult questions to answer, since the power consumption depends on many factors and the situation in general. However, we tried to capture some reference power consumption values using the evaluation board. The energy is consumed at the embedded CPU, internal custom logic, and the chip interfaces (I/O). These three are measured separately. Also, energy consumption highly depends on the activity of the signal processing. In order to capture the delta between "stand-by state" and "data transmission state", we measured them separately as well. The measurement results are shown in the table below.

It should be noted that the large amount of energy is consumed at the external interface portion (I/O column in the table)[2]. And, clock gating contributes for lowering the power consumption[3] at the "stand-by state" significantly, although there are some room to lower the power consumption further.

Table 2. Power consumption measurement result [mWatt]

	CPU	Logic[4]	I/O[5]	Total-1	Total-2
Stand-by	24.0	15.3	0.0+12.0	51.3	39.3
Stand-by (CLK gate)	2.4	10.0	0.0+12.0	24.4	12.4
Tx 145Mbps	24.0	21.0	16.0+12.0	73.0	61.0
Tx 145Mbps (CLK gate)	2.4	17.2	16.0+12.0	47.6	35.6
Rx 145Mbps	24.0	20.2	13.0+12.0	69.2	57.2
Rx 145Mbps (CLK gate)	2.4	19.0	13.0+12.0	46.4	34.4

8 Discussion and conclusion

ECMA-368 MAC protocol is introduced to capture the key technologies enabling distributed wireless networking. The protocol contains many key features to form and serve a high-speed distributed ad-hoc network. Also, the architecture, specification, and measurement results of our test LSI designed for ECMA-368 MAC are introduced. The LSI is hardwired oriented design which enables higher bandwidth signal processing with lower power consumption.

Since the ECMA-368 MAC protocol offers generic distributed wireless media coordination among devices, similar Superframe structure and the media access protocol is reused by the different wireless communication systems. ECMA-387, high rate data communication specification utilizing 60GHz, defines

[2] In Magnicours, external clock output can not be disabled, while it should be disabled. Since this can be fixed easily, the last column (Total-2) value is calculated assuming that the external clock output is disabled.

[3] Power consumption at the CPU modules highly depends on the processing load, when the clock gating is operated. In this examination, it is assumed that the minimal signal processing for beacon frames are performed.

[4] The value at the column labeled as "logic" includes consumed power by other reasons such as leakage or PLL. Leakage power was measured to be 3.5[mWatt].

[5] "+12.0" denotes external clock output consumes additional 12.0 [mWatt]. Toggle rate of the data payload is approximately 25%.

a very similar MAC protocol [13]. Since the designed LSI architecture is aimed to offer higher bandwidth signal processing, it is expected that this LSI design can be reused for these systems and deliver Gbps-order communications with marginal modification. Many of the ECMA-368 MAC protocol such as frame format, Superframe concept, TDMA channel utilization, ARQ, etc, are designed based on 802.15.3 [3], and the LSI design can be reused for 802.15.3 family systems as well, with small modifications. Further, as recently being discussed, cognitive radio systems for TV white space such as in IEEE 802.22 [14] or the like also utilize the fixed length Superframe structure with specific time window for beacon frames similar to beacon period [15]. These future systems may be also applicable systems for the utilization of this LSI, once the standardization activity is settled.

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